What is claimed is:

1. A vertical color filter detector group formed on a semiconductor substrate and comprising at least three detector layers configured to collect photo-generated carriers of a first polarity, separated by additional intervening reference layers configured to collect and conduct away photo-generated carriers of the opposite polarity, said at least three detector layers disposed substantially in vertical alignment with each other and having different spectral sensitivities as a function of their different depths in the semiconductor substrate.

2. The vertical color filter detector group of claim 1 further comprising an individual active pixel sensor readout circuit coupled to each of said at least three detector layers.

3. The vertical color filter detector group of claim 1 wherein said at least three detector layers are configured by doping to collect said photo-generated carriers of a first polarity and said plurality of reference layers are configured by doping to collect and conduct away said photo-generated carriers of said opposite polarity.

4. The vertical color filter detector group of claim 3 wherein said doping of said at least three detector layers and said doping of said plurality of reference layers is such as to cause junction isolation between adjacent ones of said detector layers and said reference layers.

5. The vertical color filter detector group of claim 3 wherein said photo-generated carriers of a first polarity are negative electrons and said photo-generated carriers of said opposite polarity are positive holes.

6. The vertical color filter detector group of claim 1 wherein each detector group includes a blue photodetector at a blue-sensitive n-type layer at the surface of the semiconductor, a green photodetector at a green-sensitive n-type layer disposed at a first depth in said semiconductor, and a red photodetector at a red-sensitive n-type layer disposed at a second depth greater than said first depth in said semiconductor.

7. The vertical color filter detector group of claim 6 wherein:

a reference layer is disposed below said blue-sensitive n-type layer;

reference layers are disposed above and below said green-sensitive n-type layer and said red-sensitive n-type layer.

8. The vertical color filter detector group of claim 6 further including:

blue active pixel sensor circuitry coupled to said blue-sensitive n-type layer;

green active pixel sensor circuitry coupled to said green-sensitive n-type layer; and

red active pixel sensor circuitry coupled to said red-sensitive n-type layer.

9. The vertical color filter detector group of claim 8 disposed in an array and associated with a column thereof and wherein;

said blue active pixel sensor circuitry has an output coupled to a blue output line associated with the column;

said green active pixel sensor circuitry has an output coupled to a green output line associated with said column; and

said red active pixel sensor circuitry has an output coupled to a red output line associated with said column.

10. The vertical color filter detector group of claim 1 further including a diffusion barrier region disposed in a layer below a lowest one of said detector layers.

11. The vertical color filter detector group of claim 1 further including a diffusion barrier region disposed in a layer below a second lowest one of said detector layers.

12. The vertical color filter detector group of claim 1 further including:

a diffusion barrier region disposed in a layer below a lowest one of said detector layers; and

a diffusion barrier region disposed in a layer below a second lowest one of said detector layers.

13. A vertical color filter detector group formed on a semiconductor substrate comprising at least six layers of alternating p-type and n-typed doped regions, PN junctions formed between abutting ones of said doped regions operating as photodiodes having spectral sensitivities that are a function of junction depth from an upper surface of said at least six layers, first alternate ones of said doped regions disposed substantially in vertical alignment with each other and serving as detector regions to collect photo-generated carriers, second alternate ones of said doped regions that are not detector regions serving as reference regions coupled to a reference potential.

14. The vertical color filter detector group of claim 13 wherein:

said detector regions comprise n-type doped regions;

said reference regions comprise p-type doped regions; and

said reference potential is ground.

15. The vertical color filter detector group of claim 14 wherein:

a blue detector region comprises a first n-type layer at an upper surface of said at least six layers;

a green detector region comprises a second n-type layer disposed below said first n-type layer; and

a red detector region comprises a third n-type layer disposed below said second n-type layer.

16. The vertical color filter detector group of claim 15 wherein:

a bottom surface of said blue detector region lies at a depth of between about 0.05 microns and about 0.5 microns from a top surface of said first n-type semiconductor layer;

a bottom surface of said green detector region lies at a depth of between about 0.5 microns and about 1.5 microns from said top surface of said first n-type semiconductor layer; and

a bottom surface of said red detector region lies at a depth of between about 1.5 microns and about 3.5 microns from said top surface of said first n-type semiconductor layer.

17. The vertical color filter detector group of claim 15 wherein:

a bottom surface of said blue detector region lies at a depth of about 0.3 microns from a top surface of said first n-type semiconductor layer;

a bottom surface of said green detector region lies at a depth of about 1.0 microns from said top surface of said first n-type semiconductor layer; and

a bottom surface of said red detector region lies at a depth of about 2.5 microns from said top surface of said first n-type semiconductor layer.

18. The vertical color filter detector group of claim 15 further including:

blue active pixel sensor circuitry coupled to said blue detector region;

green active pixel sensor circuitry coupled to said green detector region; and

red active pixel sensor circuitry coupled to said red detector region.

19. The vertical color filter detector group of claim 15 wherein said blue, green, and red pixel sensor circuitry each comprises;

a reset transistor having a source coupled to its corresponding detector region, a gate coupled to a reset signal line, and a drain coupled to a reset reference potential;

a source-follower transistor having a gate coupled to its corresponding detector region, a drain coupled to a drain supply potential, and a source; and

a row-select transistor having a drain coupled to said source of said source-follower transistor, a source coupled to a column output line, and a gate coupled to a row-select signal line.

20. The vertical color filter detector group of claim 15 wherein said blue, green, and red pixel sensor circuitry each comprises;

a reset transistor having a source coupled to its corresponding detector region, a gate coupled to a reset signal line, and a drain coupled to a reset reference potential;

a transfer transistor having a drain coupled to said source of said reset transistor, a gate coupled to a transfer signal line, and a source

a source-follower transistor having a gate coupled to said source of said transfer transistor, a drain coupled to a drain supply potential, and a source; and

a row-select transistor having a drain coupled to said source of said source-follower transistor, a source coupled to a column output line, and a gate coupled to a row-select signal line.

21. A vertical color filter detector group formed on a semiconductor substrate of a first conductivity type comprising:

a first well of a second conductivity type opposite said first conductivity type formed in the substrate;

a first epitaxial layer of said first conductivity type formed over an upper surface of said semiconductor substrate;

a second well of said second conductivity type formed in said first epitaxial layer in substantial vertical alignment with said first well;

a second epitaxial layer of said first conductivity type formed over an upper surface of said first epitaxial layer;

a shallow diffusion of said second conductivity type formed in said second epitaxial layer in substantial vertical alignment with said first well;

wherein said substrate and said first and second epitaxial regions are coupled to a reference potential.

22. The vertical color filter detector group of claim 21, further including:

a red contact region of said second conductivity type formed through said first and second epitaxial layers making an electrical contact between said first well and an upper surface of said second epitaxial layer, said red output contact region being higher than it is wide; and

a green contact region of said second conductivity type formed through said second epitaxial layer making an electrical contact between said second well and an upper surface of said second epitaxial layer.

23. The vertical color filter detector group of claim 22 wherein said first conductivity type is p-type and said second conductivity type is n-type.

24. The vertical color filter detector group of claim 21 wherein said reference potential is ground.

25. The vertical color filter detector group of claim 21 wherein:

a bottom surface of said shallow diffusion lies at a depth of between about 0.05 microns and about 0.5 microns from a top surface of said second epitaxial layer;

a bottom surface of said second well lies at a depth of between about 0.5 microns and about 1.5 microns from said top surface of said second epitaxial layer; and

a bottom surface of said first well lies at a depth of between about 1.5 microns and about 3.5 microns from said top surface of said second epitaxial layer.

26. The vertical color filter detector group of claim 21 wherein:

a bottom surface of said shallow diffusion lies at a depth of about 0.3 microns from said top surface of said second epitaxial layer;

a bottom surface of said second well lies at a depth of about 1.0 microns from said top surface of said second epitaxial layer; and

a bottom surface of said first well lies at a depth of about 2.5 microns from said top surface of said second epitaxial layer.

27. The vertical color filter detector group of claim 22 further including:

blue active pixel sensor circuitry coupled to said shallow diffusion;

green active pixel sensor circuitry coupled to said second well; and

red active pixel sensor circuitry coupled to said first well.

28. The vertical color filter detector group of claim 27 wherein said blue, green, and red active pixel sensor circuitry each comprises;

a reset transistor having a source coupled to the one of said first and second wells and said shallow diffusion associated with its color, a gate coupled to a reset signal line, and a drain coupled to a reset reference potential;

a source-follower transistor having a gate coupled to the one of said first and second wells and said shallow diffusion associated with its color, a drain coupled to a drain supply potential, and a source; and

a row-select transistor having a drain coupled to said source of said source-follower transistor, a source coupled to a column line, and a gate coupled to a row-select signal line.

29. The vertical color filter detector group of claim 27 wherein said blue, green, and red active pixel sensor circuitry each comprises;

a reset transistor having a source coupled to the one of said first and second wells and said shallow diffusion associated with its color, a gate coupled to a reset signal line, and a drain coupled to a reset reference potential;

a transfer transistor having a drain coupled to said source of said reset transistor, a gate coupled to a transfer signal line, and a source

a source-follower transistor having a gate coupled to said source of said transfer transistor, a drain coupled to a drain supply potential, and a source; and

a row-select transistor having a drain coupled to said source of said source-follower transistor, a source coupled to a column line, and a gate coupled to a row-select signal line.

30. A method for fabricating a vertical color filter detector group comprising:

providing a semiconductor substrate of a first conductivity type;

forming a first well of a second conductivity type opposite to said first conductivity type in said semiconductor substrate;

forming a first epitaxial layer of said first conductivity type over said first well and said semiconductor substrate;

forming a lower portion of a first contact plug in said first epitaxial layer to contact said first well;

forming a second well of said second conductivity type in said first epitaxial layer substantially in vertical alignment with said first well;

forming a second epitaxial layer of said first conductivity type over said second well and said first epitaxial layer;

forming an upper portion of said first contact plug and a second contact plug in said second epitaxial layer, said upper portion of said first contact plug contacting said lower portion of said first contact plug in said first epitaxial layer and said second contact plug contacting said second well; and

forming a shallow diffusion of said second conductivity type in said second epitaxial layer substantially in vertical alignment with said first well.

31. The method of claim 30 wherein forming said lower portion of said contact plug in said first epitaxial layer comprises performing multiple implants with different energies.

32. The method of claim 31 wherein at least one of said multiple implants is performed simultaneously with forming said second well.

33. The method of claim 30 wherein forming said upper portion of said first contact plug and said second contact plug in said second epitaxial layer comprises performing a single implant.

34. The method of claim 30 wherein forming said upper portion of said first contact plug and said second contact plug in said second epitaxial layer comprises performing multiple implants.

35. The method of claim 30 wherein forming said lower portion of said first contact plug in said first epitaxial layer and forming said upper portion of said first contact plug in said second epitaxial layer comprise forming a contact plug through said first and second epitaxial layers that is substantially higher than it is wide.

36. The method of claim 35 wherein forming said lower portion of said first contact plug in said first epitaxial layer and forming said upper portion of said first contact plug in said second epitaxial layer comprise forming a contact plug through said first and second epitaxial layers that is at least twice as high as it is wide.

37. The method of claim 30 wherein forming said shallow diffusion comprises forming a lightly doped drain region.

38. The method of claim 30 further including forming NMOS and PMOS transistors in said second epitaxial layer.

39. A method for fabricating a vertical color filter detector group comprising:

providing a semiconductor substrate of a first conductivity type;

forming a first well of a second conductivity type opposite to said first conductivity type in said semiconductor substrate;

forming a first epitaxial layer of said first conductivity type over said first well and said semiconductor substrate;

forming a lower portion of a first contact plug in said first epitaxial layer to contact said first well by implanting atoms of said second conductivity type a first time at a first energy level and then implanting atoms of said second conductivity type a second time, at a second energy level different from said first energy level;

forming a second well of said second conductivity type in said first epitaxial layer substantially in vertical alignment with said first well;

forming a second epitaxial layer of said first conductivity type over said first epitaxial layer and said second well;

forming an upper portion of said first contact plug and a second contact plug in said second epitaxial layer, said upper portion of said first contact plug contacting said lower portion of said first contact plug in said first epitaxial layer and said second contact plug contacting said second well; and

forming a shallow diffusion of said second conductivity type in said second epitaxial layer substantially in vertical alignment with said first well.

40. The method of claim 39 wherein forming said lower portion of said first contact plug in said first epitaxial layer and forming said upper portion of said first contact plug in said second epitaxial layer comprise forming a contact plug through said first and second epitaxial layers that is substantially higher than it is wide.

41. The method of claim 39 wherein forming said shallow diffusion comprises forming a lightly doped drain region.

42. The method of claim 39 further including forming NMOS and PMOS transistors in said second epitaxial layer.